REMARKS

The Examiner is thanked for the careful review of this Application. Claims 6, 8, and 26-35 are pending after entry of the present Amendment. Claims 1-5, 7, and 9-25 were previously cancelled. Claim 29 has been amended so as to include all the limitations of the base claim 28. Amendments do not introduce new matter.

Claim Objections:

Claims 29, 30, 33, and 35 have been objected to as being dependent upon a rejected base claim. However, claim 29 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Per the Office's instructions, the Applicants have rewritten claim 29 in independent form including the limitations of the base claim 28. As such, it is respectfully requested that objection to claims 29, 30, and 33 be withdrawn.

Rejections under 35 U.S.C. § 103(a):

The Office has rejected claims 28, 31, 32, and 34 under the 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,573,170 to Aoyagi et al. (hereinafter Aoyagi) in view of U.S. Patent No. 6,277,728 to Ahn et al. ("Ahn") as well as U.S. Patent No. 6,815,330 to Mochizuki et al. (hereinafter Mochizuki) in view of Ahn. The Applicants respectfully submit that rejection of claims under any combination of the cited prior art should be withdrawn for at least the following reasons.

The Applicants respectfully submit that neither combination of Aoyagi and Ahn nor the combination of Mochizuki and Ahn teaches the claimed invention, as suggested by the Office. In the Final Office Action, the Office has interpreted that it would have been obvious to one of ordinary skill in the art at the time of the invention to use porous dielectric material taught in Ahn as interlayer insulating material or interlayer insulation material of Aoyagi or Mochizuki, respectively. The Applicants respectfully disagree with the Office's interpretation.

The Applicants respectfully submit that the teachings of Aoyagi and Ahn are not combinable, as modifying Aoyagi using the teachings of Ahn renders the semiconductor integrated circuit of Aoyagi unsuitable for its intended purposes. For instance, Aoyagi teaches a semiconductor integrated circuit device and a technique of manufacturing the semiconductor device. Aoyagi teaches using chemical mechanical planarization to polish and flatten conductive films formed in the interlayer insulating films. However, CMP operations can be performed on the conductive films formed in the interlayer insulating layers of Aoyagi because of the silicon oxide material insulating layers and the mechanical strength provided by the silicon oxide layers. Replacing the silicon oxide interlayer insulating material of Aoyagi with the porous dielectric material of Ahn and performing CMP operations on conductive films formed in the porous dielectric materials can have

several negative outcomes. Specifically, as discussed by the Applicants on page 3, lines 5-6 of the subject application, porous dielectric materials have poor mechanical strength, and if used as insulating layers, CMP operations can cause portions of the circuit to collapse or crack, thus damaging the integrated circuits.

Still further, even if Aoyagi and Ahn were combinable (a preposition with which the Applicants disagree), the combination of the two references would not have disclosed, suggested, or taught the semiconductor device of the claimed invention. Specifically, Aoyagi does not teach using a passivation layer over the ILD layer, as defined in the claimed invention. Nor does Ahn or the combination of Aoyagi and Ahn. The Applicants respectfully traverse the Office's interpretation that the insulating film 62 shown in Figure 17 of Aoyagi is equivalent to the passivation layer of the claimed invention. Rather, the insulating layer 62 provides the same functions as all the remaining interlayer insulating layers of Aoyagi wherein interconnect metallization lines or vias are formed.

Even if the insulating layer 62 were the same as the passivation layer of the claimed invention (a preposition with which the Applicants disagree), the insulating layer 62 of Aoyagi as well as the remaining insulating layers is to be fabricated using the porous dielectric material. Under such circumstances, the transistors and active components are exposed. Therefore, the active components and transistors can be corroded, or any chemical can reach and damage the transistors and active components. Accordingly, contrary to the Office's interpretation, the semiconductor circuit resulting from combining the integrated circuit of Aoyagi and Ahn is not the same as the semiconductor device of the claimed invention.

Similarly, the Applicants respectfully submit that the teachings of Mochizuki and Ahn are not combinable, as modifying Mochizuki using the teachings of Ahn can cause the semiconductor apparatus of Mochizuki to be unsuitable for its intended purposes. By way of example, Mochizuki provides a method of manufacturing a semiconductor apparatus that includes ferroelectric capacitor. In manufacturing the semiconductor apparatus, Mochizuki uses chemical mechanical planarization to flatten the interlayer insulation films as well as the metal portions formed over the interlayer insulation films. As stated in more detail above with respect to Aoyagi, CMP can flatten the metal portions and the insulating layers because of the mechanical strength provided by the silicon oxide material used to fabricate the interlayer insulating films. When using porous dielectric material instead, as taught by Ahn, portions of the semiconductor apparatus can collapse or crack during the CMP operation, producing a damaged semiconductor apparatus.

Additionally, even if Mochizuki and Ahn were combinable (a preposition with which the Applicants disagree), the combination of the two references fails to teach or suggest the semiconductor device of the claimed invention. Particularly, Mochizuki defines multiple additional dielectric layers (layers 52 and 13, and partial layers 17, 18, 19 of t he ferroelectrics capacitor) between the interlayer insulating layers 10 and 30. Thus, even if the porous material of

Ahn were to be used to replace the insulating layers of Mochizuki, the resulting capacitive delay in the claimed invention would be less than the capacitive delay in Mochizuki, as the dielectric layers 52, 13, 17, 18, and 19 of Mochizuki remain intact.

For at least the above-stated reasons, independent claims 28 and 34 are patentable under 35 U.S.C. § 103(a) over the cited prior art. Thus, claims 31 and 32 each of which ultimately depends from claim 28 are likewise patentable under 35 U.S.C. § 103(a) over any combination of the cited prior art for at least the same reasons set forth for independent claim 28.

Indication of Allowability:

Applicant acknowledges the Allowability of subject matter in claims 6, 8, 26, and 27.

The Applicants submit that this Amendment complies with 37 C.F.R. § 1.116(b) and respectfully request that the subject Amendment be entered.

In view of the foregoing, the Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6913. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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